

VERTICALLY STRUCTURED POWER SEMICONDUCTOR COMPONENT

Cross-Reference to Related Application:

- 5 This application is a continuation of copending International Application No. PCT/DE99/02604, filed August 19, 1999, which designated the United States.

Background of the Invention:

Field of the Invention:

10 The present invention relates to a vertically structured power semiconductor component having a semiconductor body of a first conductivity type, a first main surface and a second main surface opposite the first main surface. A body zone of a second conductivity type, opposite of the first conductivity type, is introduced into the first main surface. A zone of the first conductivity type, is provided in the body zone. A first electrode makes contact with the zone of the first conductivity type and with the body zone. A second electrode is provided on the second main surface, and a gate electrode, is disposed above the body zone and is separated from the latter by an insulating layer.

25 In semiconductor power components, it is desirable to carry the largest possible current through the smallest possible

area. In order to optimize the channel width/channel length or area ratio, power semiconductor components are therefore built from a large number of cells connected in parallel, in each of which the current path runs in the vertical direction, i.e. from one main surface of the semiconductor body to its other main surface. In this way, all of the semiconductor material placed under the actual cell in question, i.e. as far as the back terminal placed on the other main surface, is used as an active volume.

It will be assumed below that the power semiconductor component is an n-channel power MOS field-effect transistor, in which the source and gate terminals are located on one main surface of the semiconductor body, the chip top, and the drain terminal is located on the other main surface of the semiconductor body, the chip bottom.

The ideas below, however, can also be applied readily to other power semiconductor components, for example insulated gate bipolar transistors (IGBT) etc.

A power semiconductor component receives the voltage applied to it through mutual depletion of neighboring p- and n-conductive regions by mobile charge carriers, so as to create a space charge zone. In an n-channel power MOS field-effect transistor, spatially fixed charges created in a p-conductive

well hence find their "mirror charges" primarily in a vertically adjacent n-conductive layer, which is normally produced by epitaxy. The maximum of the electric field always occurs at the pn junction between the p-conductive well and the semiconductor body. Electrical breakdown is reached when the electric field exceeds a material-specific critical field strength E_c : this is because multiplication effects then lead to the creation of free charge carrier pairs, so that the blocking-state current suddenly increases greatly. But since, as is known, charges are the sources of any electric field, this critical field strength E_c can be assigned an equivalent breakdown surface charge Q_c according to the first Maxwell equation. For silicon, for example, $E_c = 2.0 \dots 3.0 \times 10^5$ V/cm and $Q_c = 1.3 - 1.9 \times 10^{12}$ charge carriers cm^{-2} . The exact value of Q_c depends in this case on the level of the doping.

The voltage reduction in a power semiconductor component, which takes place in the cell array in the lower-lying volume of the semiconductor body, must also be defined toward its edge, a profile in the horizontal direction being desirable in this case. Elaborate surface-positioned equipotential structures are commonly employed in order to achieve this.

The breakdown response of power semiconductor components can be evaluated in static measurements. An "avalanche test", however, in which the switching response is also tested in

addition to the actual breakdown, is much more meaningful. In this case, different regions of the safe operating area (SOA) are run through during a test. The purpose of such measurements is to simulate the "worst case" for user applications. In order to comply with the various requirements, a power semiconductor component must, in particular, meet the below listed criteria.

First, during electrical breakdown, an impressed high current due to charge-carrier multiplication flows from the external circuit. In order to prevent destruction of the power semiconductor component, however, excessively high current densities should be avoided. Therefore, the breakdown current must be distributed as uniformly as possible across the semiconductor body, or chip. But this criterion can only be met if the actual cell array carries the major part of the breakdown current. The reason is that if the power semiconductor component breaks down in its edge structure at lower voltages than the cell array, this usually causes irreversible thermal damage to the semiconductor body, or chip. The difference in blocking voltage between the edge region and the cell array must hence be made large enough so that fabrication tolerances do not shift the breakdown towards the edge region. In general, it may hence be stated that the voltage strength of the edge region must be higher than that of the cell array.

Second, owing to fabrication tolerances, the electrical breakdown never takes place homogeneously across the entire semiconductor body, or chip. Instead, the breakdown is defined by the "weakest" cell. So in order to achieve homogenization across the cell array, the voltage at such weakest cells must become higher as the breakdown current grows, since other cells will then also enter breakdown and in turn "shift" their voltage. This distributes the "avalanche current" uniformly across the cell array. In standard power semiconductor components, the heating of the semiconductor material is normally sufficient to ensure a positive differential current/voltage response. Dynamic doping effects in which, for example, the effects of mobile charge carriers from the breakdown current are to be added to the background doping, can also facilitate such a characteristic.

In any case, the power semiconductor component should have a positive differential current/voltage response in the event of electrical breakdown.

Third, in MOS transistors, as is known, each cell contains a "three-layer system" which contains a source zone, a body zone and a drain zone, and can act as a parasitic bipolar transistor for holes created in breakdown. The base of this bipolar transistor is in this case formed by the p-conductive

well. If this base then experiences a voltage drop in the region of about 0.7 V as a result of the hole current, then the bipolar transistor is switched on and draws more and more current without any further way of controlling it, until the power semiconductor component is finally destroyed. This behavior is ultimately due to the negative temperature/resistance curve for bipolar transistors. However, such effects can be counteracted by configuration precautions. One very effective way is to avoid crossover currents at the surface, i.e. to place the electrical breakdown as deeply and centrally as possible below each cell. In other words, parasitic bipolar effects should be avoided wherever possible.

Summary of the Invention:

It is accordingly an object of the invention to provide a vertically structured power semiconductor component that overcomes the above-mentioned disadvantages of the prior art devices of this general type, in which a simple configuration is used to ensure that any electrical breakdown reliably occurs in the cell array.

With the foregoing and other objects in view there is provided, in accordance with the invention, a vertically structured power semiconductor component. The power semiconductor components contains a semiconductor body of a

first conductivity type that has a first main surface and a second main surface opposite the first main surface. A body zone of a second conductivity type opposite of the first conductivity type is introduced into the first main surface.

5 A zone of the first conductivity type is disposed in the body zone. A first electrode makes contact with the zone and with the body zone. A second electrode is disposed on the second main surface. An insulating layer is disposed on the first main surface. A gate electrode is disposed above the body zone and is separated from the body zone by the insulating layer. An intersection of the semiconductor body and the body zone defines a pn junction. The semiconductor body has a layer thickness between the pn junction and the second main surface selected such that, when one of a maximum allowed blocking voltage and a voltage just less than this, is applied between the first electrode and the second electrode, a space charge zone created in the semiconductor body meets the second main surface before a field strength created by an applied blocking voltage reaches a critical value.

20 The object is achieved in the case of a vertically structured power semiconductor component of the type mentioned at the start, according to the invention, such that the layer thickness of the semiconductor body between the pn junction
25 formed at the intersection of the semiconductor body and the zone of the other conductivity type and the second

semiconductor surface is selected in such a way that, when a maximum allowed blocking voltage, or a voltage just less than this, is applied between the first and second electrodes, the space charge zone created in the semiconductor body meets the second main surface, or just touches it, before the field strength created by the applied blocking voltage reaches the critical value E_c .

This dimensioning rule for the layer thickness of the semiconductor body between the pn junction and the second main surface is based on the following ideas.

When the power semiconductor component is in the off state, if the voltage between, for example, the source and the drain is increased stepwise, then the space charge zone spreads ever further, starting from the pn junction between the p-conductive well and the drain zone, into the n-conductive region of the drain zone. If the space charge zone meets regions with crystal defects, or intrinsically conductive noncrystalline regions, then electron-hole pairs will be emitted by these regions and, according to the potential gradient, the holes will flow through the space charge zone to the first main surface, or front, and the electrons will flow to the second main surface, or back, of the semiconductor body. This effect increases the blocking voltage and is actually to be regarded as "parasitic". If, however, the

blocking-state current increases very strongly with a small voltage change, i.e. the space charge zone reaches a very extensive region with crystal defects, then this can be utilized for breakdown. This is precisely the effect which the present invention now exploits.

The layer thickness of the semiconductor body, i.e. ultimately the chip thickness, is selected in such a way that the space charge zone meets the metallized second main surface before the critical field strength E_c has yet been reached in the bulk of the semiconductor body. It is, however, sufficient per se if the space charge zone just touches the second main surface when the critical field strength is reached, or meets this surface when the latter has been exceeded very slightly. Holes are then emitted into the bulk of the semiconductor body by the second-electrode metallization provided on the second main surface, so that the conditions for "punch-through" are satisfied. The electrons associated with the holes then pass from the metallization of the second main surface, through the external circuitry, to the voltage source that applies the blocking voltage to the source and drain.

This punch-through breakdown does in fact lower the blocking voltage of the power semiconductor component. If the configuration is appropriate, however, numerous advantages that can optimize the avalanche behavior are obtained.

First, the breakdown takes place in a reliable and defined way on the second main surface, or back, of the power semiconductor component, i.e. "far away" from the parasitic bipolar transistors near the surface. Since the holes created in the breakdown follow the potential gradient, they flow at right angles to the first main surface, i.e. at right angles to the front of the chip. Near the first main surface, the electric field is distorted as a result of the p-conductive wells to such an extent that a "funnel effect" occurs for the electric field toward the contact holes that are provided in the first main surface. This almost completely prevents any horizontally-flowing electric currents near the surface in the vicinity of the first main surface. Precautions that usually need to be taken against the parasitic bipolar effect in standard power semiconductor components therefore become unnecessary.

Second, by use of surface-positioned magneto-resistors, the space charge zone is drawn, usually at the edge of the semiconductor body, toward the first main surface, or front, and opens at the latest on a so-called "channel stopper" into a front oxide provided on the main surface. By exploiting the punch-through effect, moreover, the breakdown is automatically established under the cell array since the space charge zone extends more deeply there, and already meets the metallization

of the second main surface at smaller voltages before regions below the edge of the semiconductor body.

Third, the amplitude of the breakdown voltage is dictated primarily by the geometrical size "layer thickness of the semiconductor body", or "chip thickness", rather than by the material-dependent critical field strength E_c as in the case of previous power semiconductor components. This provides advantages, above all, in the case of so-called compensation components whose breakdown voltage generally depends parabolically on the charge balance in the semiconductor bulk, i.e. on fabrication tolerances as well. Through exploitation of the punch-through effect, the breakdown is "clamped" here and this leads to flattening of the so-called compensation parabola, and hence to homogenization of the dependency of the breakdown on the material.

The vertically structured power semiconductor component according to the invention can be produced in a relatively simple way.

After the so-called front processing on the first main surface, the wafer with the individual chips, or semiconductor bodies, is thinned to a wafer thickness which, according to the configuration of the intended power semiconductor component, allows punch-through of the space charge zone to

the back. To that end, it is possible to use thin wafer technologies as are known from the prior art (see the reference by T. Laska, M. Matschitsch, and K. Scholtz, titled "Ultrathin Wafer Technology For A New 600 V IGBT", ISRS '97, pages 361-364).

Although the thinning of a wafer entails additional costs, these can nevertheless be "neutralized". When unthinned wafers are used, it is necessary to position a heavily doped substrate below the high-impedance semiconductor volume that is used for the voltage reduction in the blocking case. This does not fulfill any necessary electrical function; it only serves, so to speak, as a support material that is intended to contribute as little as possible to the switch-on voltage in the on state, and may optionally be used as a field stop zone. However, such wafers are expensive since the layer that receives the voltage is applied on the support material by an elaborate epitaxy process. But this kind of low-impedance support material is no longer needed in thin wafer technology, so that it is possible to work with less costly substrate wafers.

Beside regions of the second main surface, i.e. the back regions, through which the space charge zone punch-through takes place and which therefore need to be doped relatively lightly (the so-called punch-through regions), it is also

necessary to define areas that ensure good contact with the metallization, i.e. ones which have low impedance. Punch-through regions hence need to be provided in alternation with terminal regions.

5

The doping concentration for the punch-through regions is dictated by the doping of the semiconductor body, i.e. the substrate doping, or it may also be varied by surface-wide back implantation. The incorporation of a weak field stop layer may possibly be advantageous in order to increase the blocking voltage of the power semiconductor component (see German Patent DE 197 31 495 C2).

To define the low-impedance terminal regions, it is necessary to structure the second main surface. This may be done, for example, by implantation through a photoresist mask. By appropriately setting the "terminal region/punch-through region" area ratio, it is possible to control the hole injection in punch-through breakdown and hence the

current/voltage characteristic in breakdown. The homogenization behavior of the breakdown across the second main surface can hence be deliberately influenced, and the point on the current/voltage curve beyond which a negative differential response is obtained, the so-called "snap-back" point, can be optimized.

It was explained above that, in the event of punch-through breakdown, the space charge zone directly adjoins the metallization of the second main surface, which results in that it is necessary to use thin wafer technology. An alternative possibility, however, is to make the space charge zone punch through onto a p-doped layer on the second main surface instead of onto the metallization. The p-doped layer hence acts as a hole injector. With this method, according to the configuration of the p-doped layer, it is possible to adapt to thicker semiconductor bodies, or wafers.

Unfortunately, a disadvantage with this approach is that, in the undepleted on state, the p-doped layer acts as a collector so that the power transistor behaves like an IGBT. In other words, parameters typical of a MOS transistor may become strongly affected.

In accordance with an added feature of the invention, the layer thickness of the semiconductor body has a specific charge density ρ in a direction z between the pn junction and the second main surface such that:

$$\int_0^W \rho(z) dz \leq 0.9 q_c$$

in which W denotes the layer thickness, and q_c denotes a critical charge quantity in the semiconductor body and is

linked to an electric field applied between the first electrode and the second electrode by Maxwell equation:

$$\vec{\nabla} \cdot \vec{E} = -4\pi\rho.$$

5

In accordance with an additional feature of the invention, the semiconductor body has heavily doped terminal regions of the first conductivity type disposed at the second main surface.

10
11
12
13
14
15
16
17
18
19
20

In accordance with another feature of the invention, a further zone of the first conductivity type is disposed in a vicinity of the second main surface.

In accordance with a further feature of the invention, the semiconductor body has punch-through regions disposed between the heavily doped terminal regions, and a current/voltage characteristic in breakdown can be controlled through an area ratio between the heavily doped terminal regions and the punch-through regions.

20

In accordance with another added feature of the invention, the semiconductor body has an edge termination and a channel stopper is disposed in an area of the edge termination.

In accordance with another additional feature of the invention, a source magnetoresistor is disposed above the first main surface.

- 5 In accordance with another further feature of the invention, a compensation region of the second conductivity type is disposed below the body zone in the semiconductor body.

10 In accordance with a further added feature of the invention, the compensation region of the second conductivity type is produced by a plurality of epitaxy and implantation operations.

15 In accordance with a further additional feature of the invention, the compensation region of the second conductivity type is produced horizontally between the first main surface and the second main surface through the same implantation openings.

- 20 In accordance with a concomitant feature of the invention, the semiconductor body has an edge region and including vertical compensation areas of the second conductivity type disposed in the edge region.

- 25 Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a vertically structured power semiconductor component, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a diagrammatic, sectional view of a vertically structured power semiconductor component according to the invention;

Fig. 2 is an enlarged sectional view of a vicinity of a second main surface in the power semiconductor component;

Fig. 3 is a sectional view of a profile of equipotential lines under an edge termination in the power semiconductor component;

Fig. 4 is a sectional view through a compensation component;
and

5 Fig. 5 is a view of an edge termination for a compensation component.

Description of the Preferred Embodiments:

As already mentioned in the introduction, the invention is described with reference to an n-channel power MOS field-effect transistor with a vertical structure. The invention is not, however, restricted to this. By reversing the conductivity types, of course, it is also possible to produce a p-channel power MOS field-effect transistor. Likewise, the invention can be used in the case of other components, for example insulated gated bipolar transistors (IGBTs).

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown an n⁻-conductive semiconductor body 1 having a first main surface 2 and a second main surface 3. A p-conductive well or body zones 4, which in turn contain n⁺-conductive source zones 5, are introduced in the vicinity of the first main surface 2. The source zones 5 are provided

with a source metallization 6, which essentially extends over an insulating layer 7 that is formed of silicon dioxide, and into which a gate electrode 8 is introduced in the region above the body zone 4.

5

n⁺-conductive terminal regions 9, which make good electrical contact with a back metallization 11, for example of aluminum, that is applied as a drain electrode D on the second main surface 3, or back, of the semiconductor body 1, are provided in the vicinity of the second main surface 3. Optionally, an n-conductive layer 10 may further be disposed in the vicinity of the back.

10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203

main surface 3 before the field strength created by the applied blocking voltage reaches a critical value E_c .

The critical value E_c of the field strength is linked to a

5 charge density ρ by the Maxwell equation

$$\vec{\nabla} \cdot \vec{E} = -4\pi\rho, \quad (1)$$

so that a relationship with a critical breakdown charge q_c can be derived:

$$\int_0^W \rho(z) dz = q_c. \quad (2)$$

According to the invention, the layer thickness W should then be selected in such a way that the space charge zone reaches the second main surface 3 before the field strength takes on the critical value E_c . In other words, the integral in Equation (2) should, for example, reach at most the value $0.9 q_c$ so that, in the vertically structured power semiconductor component according to the invention, the following equation is satisfied:

$$\int_0^W \rho(z) dz \leq 0.9 q_c. \quad (3)$$

Fig. 3 shows an edge termination of a power semiconductor component having a p^+ -conductive source zone 15, a source magnetoresistor 16 and a channel stopper 13, which is provided with a magnetoresistor 26 and is n^+ -doped. The semiconductor body 1 is n^- -conductive as in the exemplary embodiment above. Further, the profile of equipotential lines 14 can be seen from Fig. 3.

As shown in Fig. 3, the breakdown is fixed below the cell array in the power semiconductor component according to the invention, since the space charge zone (see the equipotential lines 14) extends more deeply there, and hence already meets the metallization on the second main surface 3 at smaller voltages before this happens for regions below the edge.

Fig. 4 schematically shows a compensation component, in which an n -conductive epitaxial layer 21, which contains a p -conductive well 22, a p^+ -conductive body zone 23 and an n^+ -conductive source zone 25, is provided on an n^+ -conductive substrate 20. Further, a p -conductive "column" 24 which, for example, is produced by several epitaxies in combination with implantations, is provided for "compensation".

In the power semiconductor component, vertically extending p -conductive and n -conductive areas, so-called "columns", are disposed next to one another in the active volume below the

source metallization 6. In the on state, there is hence an uninterrupted low-impedance conductivity path from the source terminal, or the metallization 6, to the drain terminal, or the n^+ -conductive substrate 20.

5

Each of the two charge areas or "columns" must contain only a fraction of the breakdown surface charge, seen in the horizontal direction, so that the horizontal surface charge is smaller than the critical charge q_c . In the blocking case, the voltage is received by the power semiconductor component through mutual depletion of neighboring p-conductive and n-conductive areas. In other words, the charge carriers of one area electrically "compensate" for those of the oppositely charged area. In the individual planes, at low voltages, this leads to an electric field which is primarily directed horizontally.

As the voltage between the source and the drain rises, an increasing part of the volume becomes horizontally depleted, until at least one of the two "columns" disposed next to each other is fully exhausted of charge carriers. A horizontal electric field E_h has then reached a maximum value E_{Bh} . As the voltage rises further, the depletion of the n^+ -conductive substrate 20, or of deeper-lying surface-wide epitaxial layers, or of the p-conductive well 22, begins so that a vertical electric field E_v then builds up.

Breakdown is reached when the vertical field reaches a value E_{Bv} for which:

$$E_c = |\vec{E}_{Bv} + \vec{E}_{Bh}| \rightarrow E_{Bv} = \sqrt{E_c^2 - E_{Bh}^2} . \quad (4)$$

If the dimensions of the individual cells are appropriate, the horizontal field E_{Bh} only takes on relatively low values even if the columns are heavily doped, which results in a low switch-on resistance R_{on} , so that the vertical field E_{Bv} is of the order of magnitude of E_c . Therefore, in spite of a low switch-on resistance R_{on} , such a compensation component makes it possible to block high voltages.

When the doping conditions in the columns are appropriate, it is also possible to configure compensation elements in such a way that there is an almost linear dependency between the blocking voltage and the switch-on resistance.

The application of the present invention to compensation components offers the below listed special advantages.

Since the punch-through breakdown takes place in the cell array rather than at the edge, the requirement that the edge needs to block more voltage than the cell array can be

eliminated. The structure of the cell array may therefore be continued unchanged as far as the edge. Therefore, the implantation openings in the individual epitaxial layers no longer need to differ between the cell array and the edge, as in the case with previous standard compensation components.

A preferred field of application of the invention hence involves compensation components in which columnar, vertically extending and p-doped compensation areas 27 (corresponding to the "column" 24) are incorporated, for example, in the n-conductive semiconductor body 1. An edge structure for this, having a magnetoresistor 28 and the channel-stopper magnetoresistor 26, is shown in Fig. 5.

Another advantage of the present invention is the fact that, in the event of breakdown in the vicinity of the second main surface, or back, only holes are injected into the semiconductor bulk. These, however, exhibit much weaker capacities for multiplication than electrons that would be created in the semiconductor body, together with the holes, in the event of standard field breakdown.